Design, Fabrication, and Evaluation of 2- and 3-Bit GaAs MESFET Analog-to-Digital Converter IC's

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Abstract —**The analog-to-digital converter (A/D) is a critical component of a signal processing system. GHz-rate A/D's will be required in many future systems. While Si bipolar based A/D's can easily meet 4–6-bit resolution requirements, excessive power dissipation (1 W per bit) limits their operation to 100–400-MHz sampling rates. Recently, GaAs MESFET's have demonstrated high frequency operation with relatively low power dissipation. This paper describes the design of 2- and 3-bit A/D's using GaAs MESFET's. Monolithic integrated A/D circuits were fabricated and successfully operated at gigahertz sampling rates. This sampling rate is the highest reported for any A/D technology at room temperature. The power dissipation is 150–200 mW per bit. With further improvements in comparator sensitivity, the design can be extended to 4-bit A/D for GHz rate operation.**

I. INTRODUCTION

SYSTEMS of the 1980's and beyond will require signal and data processing at gigabit rates. Analog-to-digital converters (A/D) are a critical part of most signal processing systems. High resolution and low conversion rate A/D's are required in communication systems while low resolution and high conversion rate A/D's are required for RADAR signal processing. Griffiths [1] has shown that major improvements can be made in RADAR system performance if 2- or 3-bit A/D's operating at GHz rates are available. Degraaf *et al.* [2] have reported silicon bipolar based A/D's operating in the 300–400-MHz range. The power dissipation in these circuits is 1.0 W per bit and there is no possibility of extending the sampling rate. A/D's using other silicon devices (e.g., MOS) operate at very low conversion rates. Therefore, it is necessary to study the suitability of other semiconductor devices and circuit configurations for high-speed A/D applications. Upadhyayula [3], [4] proposed GaAs MESFET comparators for gigabit-rate analog-to-digital converter applications. Based on this principle, 2- and 3-bit A/D circuits were designed. The design, fabrication, and evaluation of these A/D's are described in this paper. The performance of 2- and 3-bit A/D's was studied at sampling rates as high as 1.0 GHz. The smallest-width sample/hold type input digitized is 500–600 ps.

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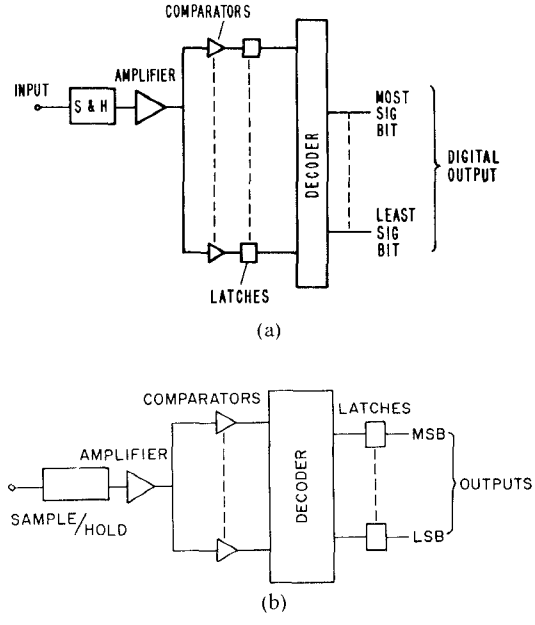

Fig. 1. Parallel comparator A/D architecture for realizing the maximum conversion rate (a) Conventional arrangement. (b) Modified arrangement when decoding time is relatively short compared to the comparator response time

II. DESIGN CONSIDERATIONS

Gordon *et al.* [5] have published an excellent review article on analog-to-digital converters. Flash converter or parallel comparator type A/D architecture of Fig. 1(a) is recommended for high-speed and medium resolution A/D's. When implemented with GaAs FET's, the decoder response time is of the order of 100–200 ps. The decoder circuits can, therefore, be used ahead of the latches as shown in Fig. 1(b). This arrangement significantly reduces the number of latches required, resulting in a substantial lowering of dc power consumption. This is the architecture selected in our A/D development. Some preliminary work is being carried out on sample and hold (S/H) circuits following Saul [6], but this work is beyond the scope of the present paper. Standard d-type flip flops are used for latches. The following section describes the design of the comparators and decoders.

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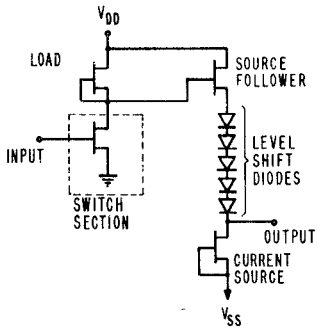


Fig. 2. GaAs MESFET comparator.

A. GaAs MESFET Comparators

The number of comparators required for an n-bit parallel comparator architecture is $(2^n - 1)$. Two- and three-bit resolution, therefore, requires 3 and 7 comparators, respectively. The quantization step (Q) for the comparator threshold voltages is given by

$$Q = \frac{\text{full-scale voltage}}{2^n - 1}.$$

Assuming a full-scale voltage of the order of 1.6 V, the Q values used are about 0.4 and 0.2 V for 2- and 3-bit resolution, respectively. For proper operation, the quantization step must be equal to or less than twice the comparator overdrive voltage. Overdrive voltage (ΔV) is the voltage change required at the threshold value for the comparator output to make the transition from logic LOW to HIGH or vice-versa. This overdrive voltage is a characteristic of the comparator architecture and technology and determines the ultimate A/D resolution.

A MESFET comparator circuit is shown in Fig. 2. The principle of operation and design procedures for GaAs MESFET comparators have been discussed in a recent paper [4]. A brief discussion is included here. When a voltage ΔV is applied at the MESFET comparator input, the drain–current changes by $\Delta I = g_m \Delta V$ which provides the charging or discharging current for the load. The load on the comparator is the input capacitance of the source follower and is typically 0.03 pF. The current required for charging or discharging is thus given by

$$\Delta I = C\frac{\Delta V}{\Delta t}.$$

The voltage change at the comparator output is about 3 V. For the switching transition to occur in 150 ps, a current change of 0.6 mA is needed. The size of the switching transistor in the comparator is determined by this current requirement. An FET with 6-mS transconductance will bring the 0.6-mA current charge for $\Delta V = 0.1$ V. This value for ΔV is one-half of the value of the quantization step (Q) which ensures proper comparator operation.

The minimum size of the switch FET in the comparator is determined using the graphical design procedure of Fair [7]. An $8\text{–}10 \times 10^{16}$ cm^{-3} doping density is used for GaAs FET's. The minimum gate length possible with optical lithography and contact printing is 1.0 μm. From Figs. 4 and 6 of Fair [7], $I_{DSS} = 17.5\text{–}20$ mA and $g_m = 7.0\text{–}7.5$ mS for a 100-μm wide device with 5–6 channel pinch-off voltage. Thus a 100-μm FET satisfies the requirements for the switch FET. The size of the load transistor is computed from the threshold level for the comparator. At the threshold levels, the switching transistors in the comparators will have different drain–current values and can be calculated from the relation

$$I_{DS} = I_{DSS}\left(1 - \eta^{1/2}\right)/\left(1 - \eta_S^{1/2}\right)$$

where

I_{DSS} is the drain saturation current

$\eta_S = \dfrac{V_B}{V_p}$, $\eta = \dfrac{V_B + V_G}{V_p}$

V_B is the built-in Schottky-barrier voltage

V_G is the external gate voltage (comparator threshold–voltage level in our case)

V_p is the pinch-off voltage.

The widths of the load transistors for the comparators have been chosen such that their drain saturation currents (I_{DSS}) for $V_G = 0$ equals the saturation currents computed above for different threshold voltage levels.

As discussed earlier, the quantization step (Q) is equal to 0.4 V for a 2-bit A/D. The threshold levels for the three comparators are, therefore, 0.4, 0.8 and 1.2 V, respectively. The quantization step (Q) is 0.2 V for the 3-bit A/D and the threshold levels for the comparators are thus 0.2, 0.4, 0.6, 0.8, 1.0, 1.2 and 1.4 V. The ratio of the width of the load FET to that of the switch FET for various comparators in the 2- and 3-bit A/D's were calculated from the above relation and summarized in Tables I and II. The

TABLE I
COMPARATOR DESIGN PARAMETERS FOR A 2-bit A/D

	Width of the Load FET/Width of the Switch FET			
Comparator	V_B = 0.4 V		V_B = 0.6 V	
Threshold	V_p = 5.0 V	V_p = 6.0 V	V_p = 5 V	V_p = 6 V
0.4 V	0.837	0.856	0.845	0.865
0.8	0.711	0.745	0.720	0.756
1.2	0.606	0.652	0.612	0.661

TABLE II
COMPARATOR DESIGN PARAMETERS FOR A 3-bit A/D

	Width of the Load FET/Width of the Switch FET			
Comparator	V_B = 0.4 V		V_B = 0.6 V	
Threshold	V_p = 5.0 V	V_p = 6.0 V	V_p = 5.0 V	V_p = 6.0 V
0.2 V	0.9114	0.9218	0.9180	0.9285
0.4	0.8366	0.8558	0.8458	0.8654
0.6	0.7708	0.7977	0.7805	0.8084
0.8	0.7113	0.7452	0.7204	0.7560
1.0	0.6566	0.6969	0.6645	0.7073
1.2	0.6056	0.6519	0.6120	0.6614
1.4	0.5578	0.6097	0.5623	0.6181
1.6	0.5125	0.5698	0.5151	0.5769

TABLE III
DESIGN PARAMETERS FOR FET COMPARATORS

Operating Bias ~ + 7 5 V and -5 0 V	Power Dissipation/Comparator =
Device Pinch-Off Voltage ~ 5 0 V	150-175 mW
Switching Speed ~ 100-150 ps	Width of the Switching Transistor
Gate Length ~ 1 0 μm	~100 μm
Doping density ~ 1.0×10^{17} cm^{-3}	

Schottky-barrier voltage (V_B) and the channel pinch-off voltage (V_p) are used as parameters.

The ratio of the width of load FET to the width of the switch FET determines the threshold levels and this ratio must be maintained to a high degree of accuracy. There is no need, however, to control the widths of individual FET's very accurately.

From Tables I and II note that the ratio of the widths is less sensitive to the Schottky-barrier built-in potential. Since photolithographic techniques allow geometry control to within a micrometer, these comparators are realizable. The threshold voltage is more sensitive to the variation in pinch-off voltage, however, and this must be kept in mind during fabrication.

FET comparator design parameters are summarized in Table III. These parameters are the optimum values. Comparators' threshold values will change with variations in the device parameters.

B. GaAs MESFET Decoder

Comparator outputs must be converted to provide bit outputs. The bit outputs may be in either binary or gray code format. The outputs of the comparators are designated by numerals $1,2,\cdots,7$ and their complements are designated by a bar above the numerals (e.g., $\bar{2},\bar{4}$, etc.). Binary outputs are provided for 2-bit A/D's. However, gray code outputs are provided for 3-bit A/D's because of the simplicity and faster response of the decoder logic circuits for gray code. The logic equations used in our implementation are

Binary Outputs for 2-bit A/D's

$$2^0 = 1\cdot\bar{2}+3 \text{-----(bit 2)}$$

$$2^1 = 2 \text{----------(bit 1)}$$

and

Gray Code Outputs for 3-bit A/D's

$$2^0 = 1\cdot\bar{3}+5\cdot\bar{7} = \overline{(\bar{1}+3)\cdot(\bar{5}+7)} \text{---(bit 3)}$$

$$2^1 = 2\cdot\bar{6} = \overline{(\bar{2}+6)} \text{ ---------- (bit 2)}$$

$$2^2 = 4 \text{ ---------- (bit 1)}$$

Simple NAND/NOR gates can be used to implement the decoding logic. The design of such logic circuits has been discussed in the literature [8]–[10]. We have selected buffered FET logic (BFL) for our circuit implementation because of its versatility and higher speed. To minimize power dissipation, a channel pinch-off voltage of about 2.0 V is used for the logic circuits. Assuming 0.9–1.0-V drop across the forward-biased diodes, a three-diode level shifting circuit is required in the source-follower section.

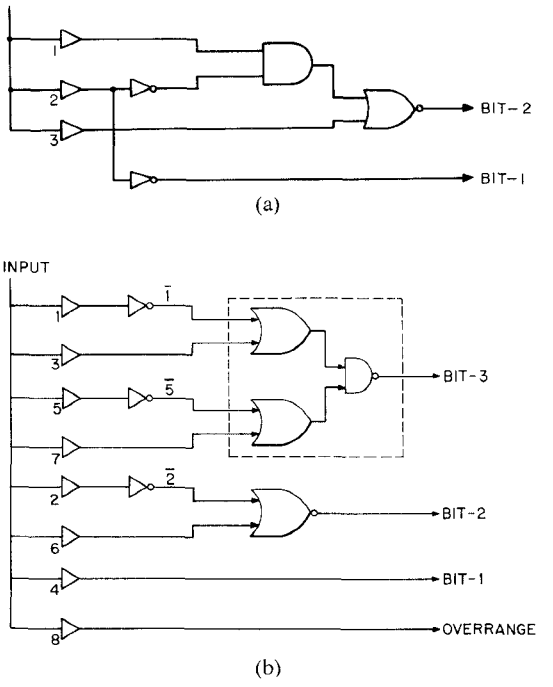


Fig. 3 Schematic of proposed MESFET A/D circuits. (a) 2-bit A/D with binary coded output. (b) 3-bit A/D with gray code output.

The 2- and 3-bit A/D circuits are schematically shown in Fig. 3.

C. Computer Simulation and Circuit Analysis

The circuit model [11] for the MESFET is contained in a subroutine developed for use with R-CAP, a powerful circuit simulation program. This model accurately describes the GaAs drain MESFET current–voltage characteristics, includes transit-time delay effects, and provides voltage dependent gate–source capacitance. MESFET parameters not directly measurable are acquired from two-dimensional MESFET simulation [11].

For A/D's the critical parameters are comparator threshold levels, overdrive voltage, and response time. A slowly varying input voltage was used to determine threshold characteristics. Computer-simulated response of the comparators for 2-bit A/D is shown in Fig. 4. Note that the comparator thresholds agree with design values. The overdrive voltage is seen to be about 0.1 V for the MESFET comparators. The value of the overdrive voltage limits quantization step size and hence the ultimate A/D resolution.

The A/D transient response was studied by applying a pulse input to the circuit. The rise and fall times of the pulse are 80–100 ps and the pulse width is 400–600 ps. The longest settling time in the 3-bit A/D is associated with bit-3, the lowest order bit. In the worst case, as many as four comparators may change states before an output is produced. Circuit simulation showed that a decoding logic sequence of INVERTOR-OR-NAND gates resulted in shorter settling time than an INVERTOR-AND-NOR logic sequence.

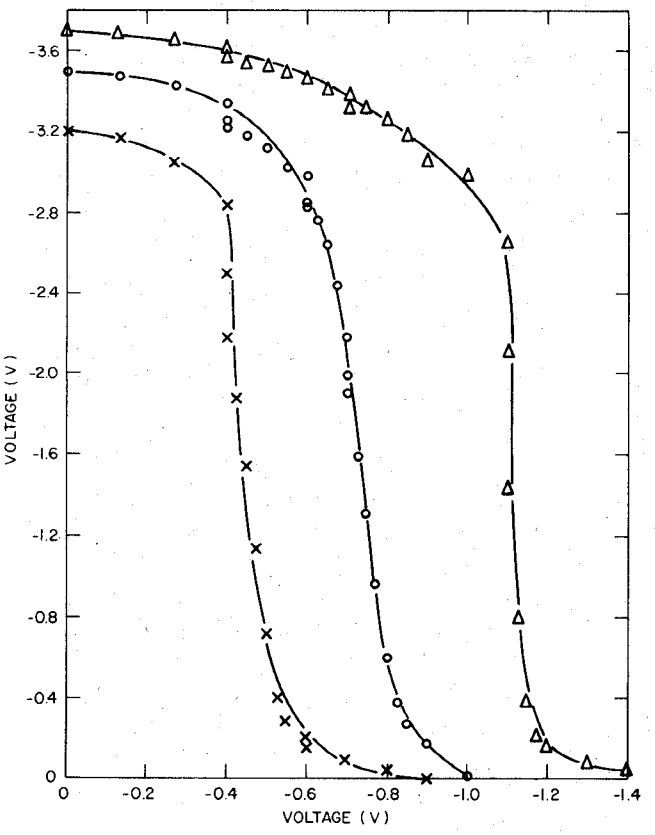


Fig. 4. Computer simulation of the threshold characteristics of comparators designed for 2-bit A/D's. Threshold levels are −0.4, −0.8, and −1.2 V. Overdrive voltage is 80–100 mV.

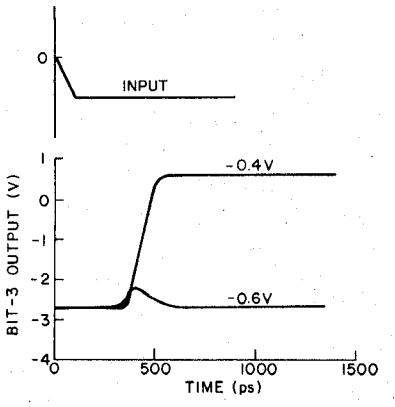


Fig. 5. Simulated response of LSB (bit-3) in 3-bit A/D for input pulse amplitudes of −0.4 and −0.6 V.

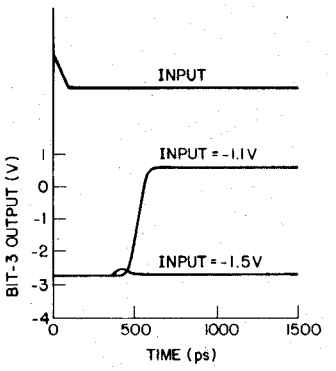


Fig. 6. Simulated response of LSB in 3-bit A/D for input pulse amplitudes of −1.1 and −1.5 V.

Fig. 3(b) shows the INVERTOR-OR-NAND logic configuration for the bit-3 output. The inverters follow the fastest switching comparators and help balance the parallel signal delays. The simulation is made assuming all MESFET's in the comparators and in the decoding section have 5- and 3-V pinch-off voltage, respectively. Characteristics of our 1-μm gate length GaAs MESFET's have been assumed.

Simulated transient response of bit-3 is shown in Figs. 5 and 6 for four different input voltages. In Fig. 5 when the input is −0.4 V, comparator 1 thresholds and produces an output logic HIGH. When the input is −0.6 V, comparators 1 and 3 threshold and the output is logic LOW. In Fig. 6 when the input is −1.1 V, comparators 1, 3, and 5 threshold and produce an output logic HIGH. When the input is −1.5 V, comparators 1, 3, 5, and 7 threshold and produce an output logic LOW. The bit-3 output can be seen to settle after about 500 ps. The longest settling time for any input voltage level is about 550 ps. This circuit is, therefore, capable of processing samples at the rate of 1 GHz or higher.

III. Integrated Circuit Fabrication

Two- and three-bit A/D IC's were fabricated using standard optical photolithography and contact printing techniques. The majority of the IC's were fabricated on wafers expitaxially grown on semi-insulating GaAs substrates. The epitaxial layer thickness was about 0.6 μm and doping density $0.8–1.0\times10^{17}$ cm^{-3}.

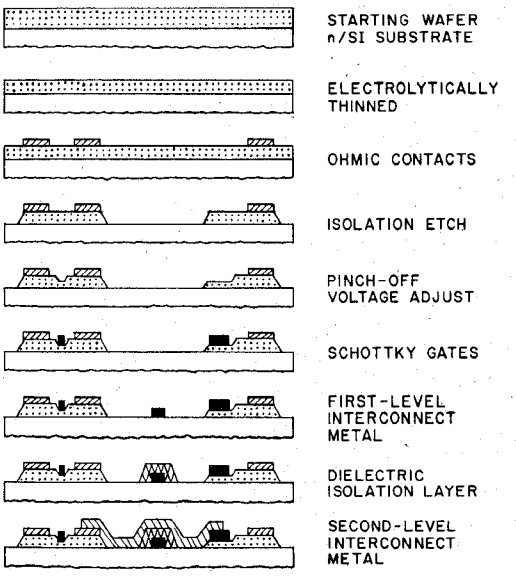


Fig. 7. Process schedule developed for GaAs IC fabrication.

The process schedule developed for the fabrication of GaAs IC's is illustrated in Fig. 7. The critical steps are briefly discussed. The starting wafers are electrolytically thinned to the limit by anodic oxidation and oxide stripping [12] to obtain uniform nt product across the wafer. Sintered Au: Ge/Ni/Au ohmic contacts are used. The

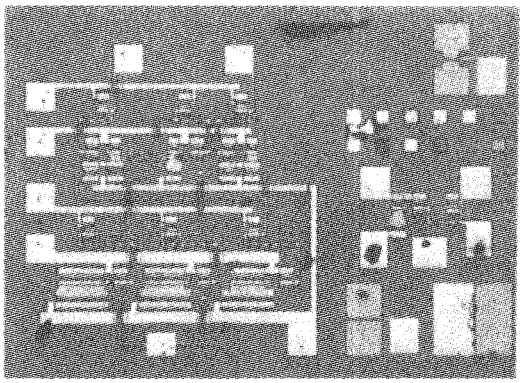
typical specific contact resistance is about 1×10^{-5}–$2\times10^{-6}\ \Omega\cdot\text{cm}^2$. For the 10-$\mu$m × 10-$\mu$m ohmic contacts on the IC, ion etching yielded much smoother surfaces than metal liftoff. Device isolation is achieved by mesa etching. Because of the small size of the MESFET's used to obtain low-power dissipation, ion etching was preferred to chemical etching. Recessed-gate structures were used for MESFET's. Pinch-off voltages were adjusted during the gate-recess process. In this procedure, the channel under the gate is selectively etched until the final current is a specific fraction of the open channel current. This procedure enables the adjustment of the pinch-off voltages for logic-array and comparator FET's to about 1.5–2.0 V and 5–6 V, respectively. Ti/Pd/Au Schottky barriers were used for MESFET gates and level shifting diodes.

Two-level interconnections are required for completing GaAs IC's. Dielectric layers were used for isolation in defining the crossovers. Plasma deposited Si_3N_4 was found to have a poor step coverage. Also, the etch rate is very much dependent on its composition resulting in severe undercutting. Dupont PI-2555 polyimide with 3 : 1 dilution by weight in pyrrolydinone was found to provide excellent isolation layers for GaAs IC's. This polyimide requires low temperature curing (~ 200°C) and can be patterned by either oxygen plasma or chemical etching. Both these processes are compatible with our GaAs IC fabrication schedule. The smallest isolation island defined was 7.5 μm × 10.0 μm.

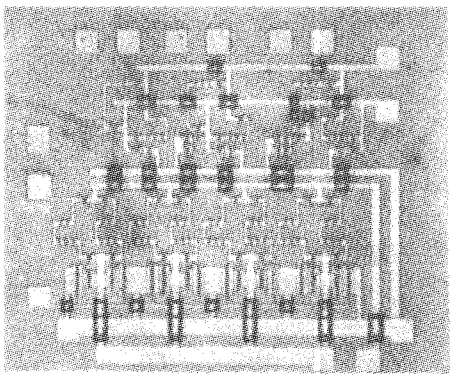
Ti/Pd/Au metallization was used for interconnections. The minimum width of the interconnect lines was 3 μm and the metal thickness is 0.7–1.0 μm. Photomicrographs of 2- and 3-bit A/D IC's are shown in Fig. 8. The chip size is 1.3 mm × 1.0 mm for 2-bit and 1.5 mm × 1.3 mm for 3-bit IC's. The gate length is 1.0 μm. The smallest MESFET width (in the logic section) is 10 μm. There are 26 MESFET's and 24 diodes in the 2-bit circuit and 57 MESFET's and 55 diodes in 3-bit circuits.

IV. Experimental Results

The A/D IC's fabricated consist of the comparators and the coding logic. Sample-and-hold circuits and the digital-to-analog (D/A) circuits were not incorporated. Such circuits operating at 1.0-GHz sampling rates are not available. The IC's were tested as follows. DC biases were independently optimized for the comparator and logic circuits. A variable input (0 to −1.6 V) was fed to the comparators and the corresponding binary or gray-coded outputs were monitored. The IC performance was then studied from dc through GHz sampling rates. The two- and three-bit converters were tested with input pulses as narrow as 0.5–0.8 ns. Such input pulses correspond to the sample-and-hold pulses seen by the comparators. Two-bit A/D IC's were extensively studied. Some results were recently reported [13]. Three-bit A/D IC's are currently being evaluated and some of these results were reported separately [14]. A complete summary of results on 2- and 3-bit A/D's is presented below.



(a)



(b)

Fig. 8. Photomicrograph of fabricated integrated circuits. (a) 2-bit A/D. (b) 3-bit A/D.

A. Two-Bit A/D's

The response of a 2-bit A/D to a dc input is shown in Fig. 9. Comparator thresholding and output encoding are clearly evident. The measured quantization step is 0.55 V, slightly larger than the design value (0.4 V). This difference is due to the higher pinch-off voltage on the devices. The threshold for the first comparator is 0.2 V instead of 0.4 V. This offset error is discussed later. The response of A/D to a wide (90 ns) input pulse is shown in Fig. 10. The input pulse rise time is 10–20 ns. Due to this finite rise time, the threshold of comparator 1 is reached much earlier than that for comparator 2. Correspondingly, a spurious output is observed at the 2^0-bit for a short period of time when the input is at or above the second comparator threshold. This spurious output disappears after the second comparators responds. The response of A/D to 1.0-ns wide input pulses is shown in Fig. 11. The general features of the output are similar to that for the wide input pulse. This demonstrates that the circuits function up to a GHz sampling rate. The performance of the circuit to 0.5–0.7-ns sample/hold type input is shown in Fig. 12. The response is satisfactory. This result is in good agreement with computer simulations and confirms that the circuit can operate above 1.0-GHz sampling rate.

B. Three-Bit A/D

Gray code outputs are provided in 3-bit A/D's. Computed bit-outputs and the corresponding gray code for

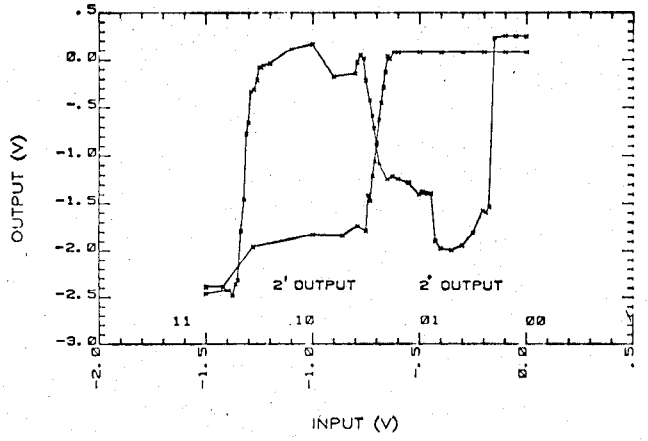


Fig. 9. Measured response of 2-bit A/D for dc input voltage.

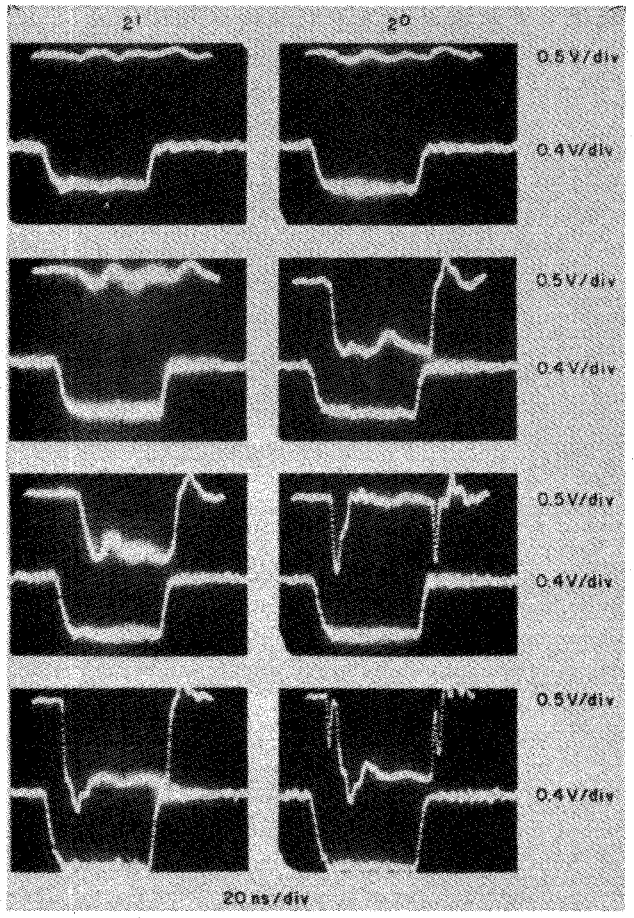


Fig. 10. Performance of 2-bit A/D to a wide (90 ns) pulse input for four different voltage levels. In each frame, the bottom trace is the input and the top trace the output.

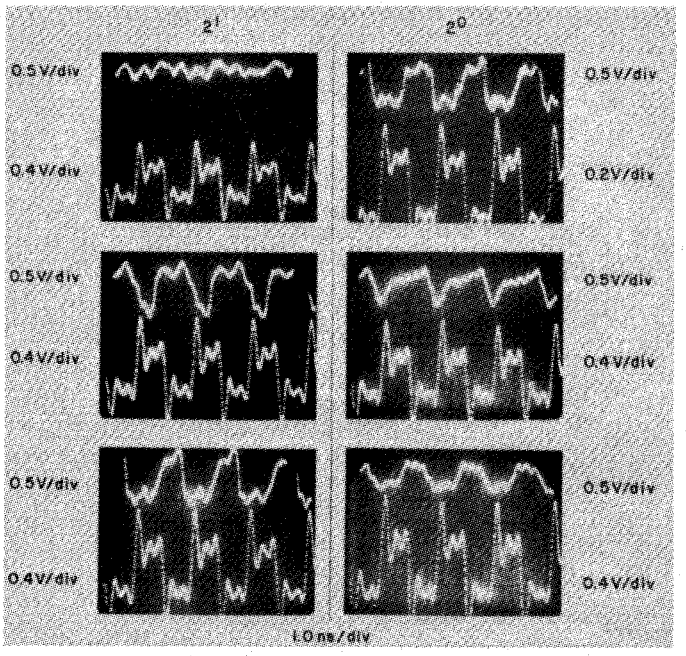


Fig. 11. Performance of 2-bit A/D to a narrow (1 ns) pulse input for three different voltage levels. In each frame, the bottom trace is the input and the top trace the output.

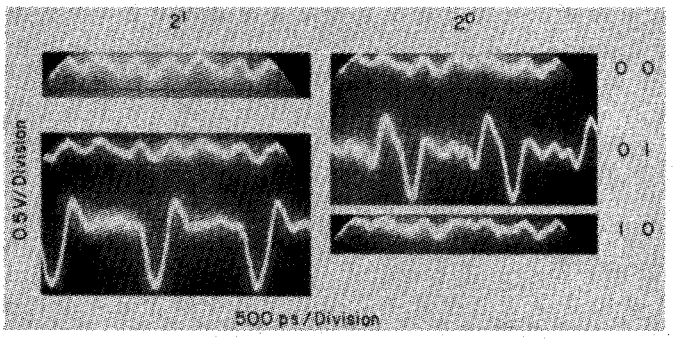


Fig. 12. Outputs of 2-bit A/D to 600-ps wide pulses with four different voltage levels.

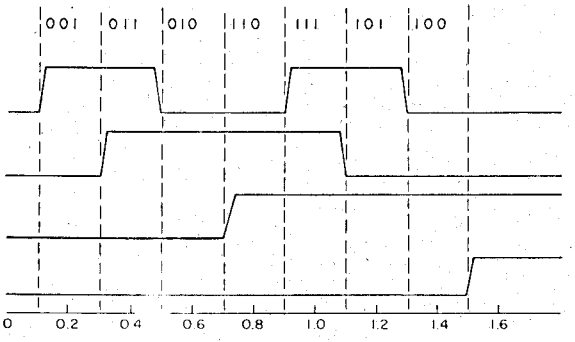


Fig. 13. Computed bit outputs for 3-bit A/D for 0− to −1.6-V input.

input signals from 0–1.6 V is shown in Fig. 13. An overrange bit is also provided. Measured response of the 3-bit A/D to a dc input is shown in Fig. 14. The measured result closely resembles the computed response. However, some off-set errors were observed in the response characteristic. Performance of the 3-bit A/D was also measured for pulse inputs. The response of bit-3 (LSB) output for a wide pulse input is shown in Fig. 15. When the input is below threshold for comparator 1, the output is zero (Fig. 15(a)). When the input is increased above the threshold level, a logic "1" is produced (Fig. 15(b)). Bit-3 response of 3-bit A/D for a 600–700-ps wide pulse is shown in Fig. 16. This result demonstrates that the response time of the comparators and coding logic is less than 600 ps. As discussed in the section on simulation, the LSB has the

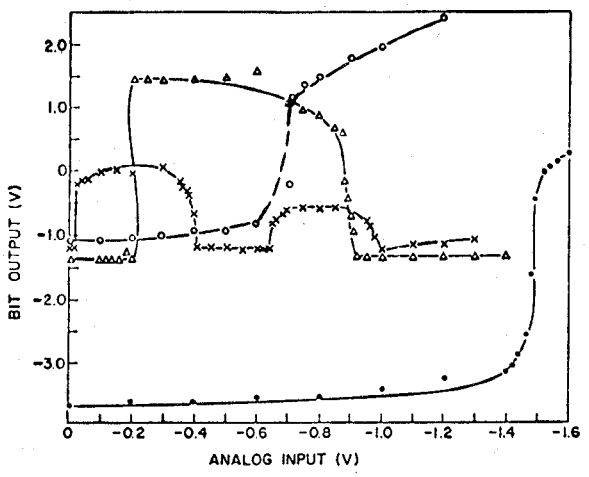


Fig. 14. Measured response of 3-bit A/D to dc input.

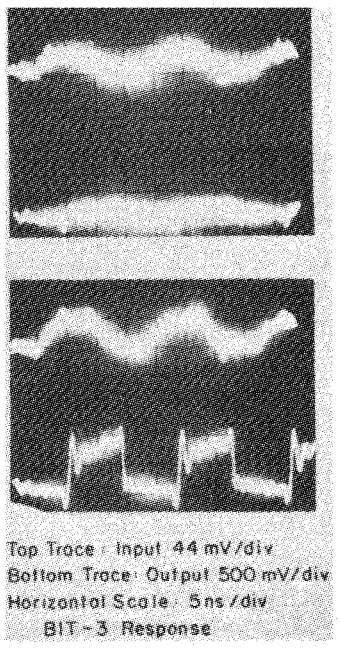


Fig. 15. Bit-3 response when a wide pulse input is applied to 3-bit A/D.

longest settling time. The LSB settling time is, therefore, less than 600 ps confirming the suitability of these circuits for GHz rate operation.

V. Discussion

Satisfactory performance of both the 2-bit and 3-bit A/D IC's was demonstrated. These IC's were successfully operated at GHz sampling rates. This sampling rate is the highest reported in the literature for devices operating at room temperature. Work is underway to decrease the overdrive voltage from 80–100 to 40–50 mV. This will improve comparator sensitivity and lead to a 4-bit A/D implementaton. Before these GaAs MESFET A/D's are considered for any system applications, other parameters have to be investigated. Therefore, we also studied off-set and gain (or scale factor) errors and these data are presented below.

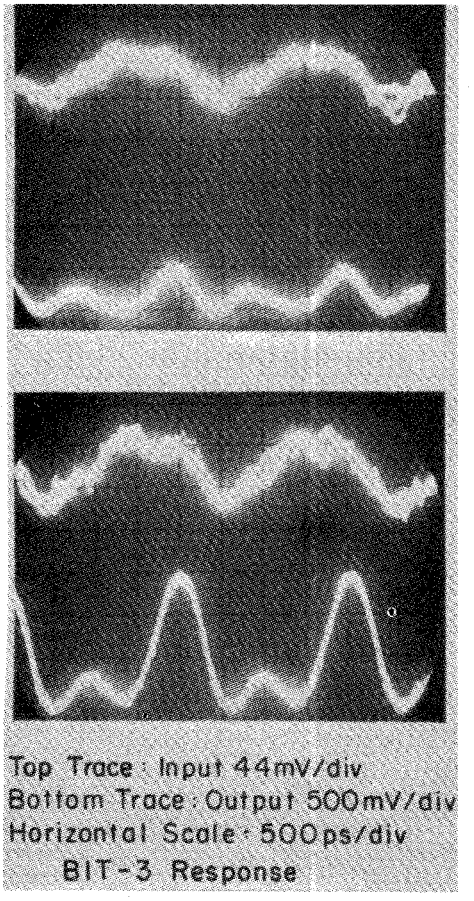


Fig. 16. Bit-3 response when a 600-ps pulse input is applied.

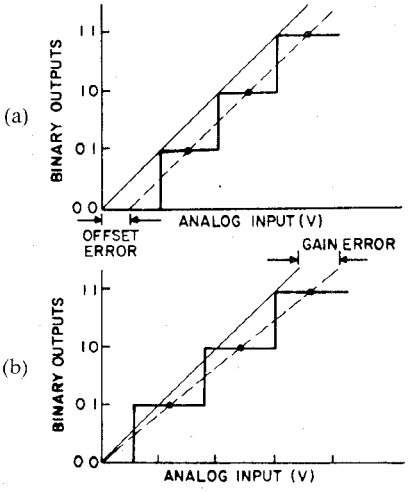


Fig. 17. Typical transfer functions of A/D's. (a) Shows scale factor (or gain) error. (b) Shows off-set error.

A. Scale Factor or Gain Error

Transfer functions of a typical A/D are shown in Fig. 17. Assume that the solid lines correspond to the ideal design values and the dashed lines correspond to the measured values. In Fig. 17(a) the slopes of the two transfer functions are different. The difference in full-scale

TABLE IV
COMPARATOR THRESHOLD AS A FUNCTION OF PINCH-OFF VOLTAGE

	COMPARATOR THRESHOLD VOLTAGE (V_p)		
1/K	V_p = 6 V	V_p = 5 V	V_p = 4 V
0.845	0.47	0.40	0.32
0.720	0.946	0.80	0.649
0.612	1.429	1.20	0.963

TABLE V
COMPARATOR THRESHOLD AS A FUNCTION OF V_B
(Pinch-off Voltage is 5 V)

	Threshold Voltage	
1/K	V_B = 0.6 V	V_B = 0.4 V
0.845	0.40	0.376
0.720	0.80	0.770
0.612	1.20	1.174

values between the actual transfer function and the ideal is defined as the gain or scale factor error and is expressed in percentage. In 2-bit A/D, we have measured gain error as high as 30 percent. We believe that the gain error is due to variations in the pinch-off voltage. Table IV shows variations of comparator threshold as a function of channel pinch-off voltage. Our design was based on $V_p = 5.0$ V. A ± 20-percent variation in V_p produces a ± 17-percent change in quantization levels and introduces the same error in the gain function. We measured pinch-off voltages as low as 3.6 V and as high as 7.0 V. We believe that the changes in V_p are responsible for scale factor (or gain) error in GaAs MESFET A/D's. This error can be minimized by a more stringent control on the pinch-off voltages during fabrication. In principle, the gain of the post amplifier after the S/H circuit can be adjusted to compensate for this error.

B. Off/Set Error

In Fig. 17(b), the A/D transfer function is shifted to the right from the ideal function. The analog value by which the transfer function fails to pass through the origin is termed the off-set error. This is expressed in millivolts. We measured off-set errors of the order of 0.18–0.20 V. The off-set errors in GaAs MESFET comparators can be attributed partly to variations in Schottky-barrier, built-in potential (V_B). Changes in comparator threshold voltage (V_B) for a corresponding change in built-in potential (V_B) is given in Table V. Here, the pinch-off voltage (V_p) is fixed at 5 V. The step size is still 0.4 V. The threshold values, however, are shifted by about 26–30 mV. From the design equations, it can be seen that the off-set error due to changes in V_B increased with pinch-off voltage. For example, when V_p is 7.0 V, the off-set error due to V_B will be about 40 mV. Variations exist in MESFET characteristics (i.e., I_{DSS}, V_p, g_m, etc.) on a microscopic scale. Such variations may also be responsible for off-set errors. Off-set errors can be corrected by adjusting the dc level at the output of the post amplifier.

VI. CONCLUSIONS

Comparators and decoding logic circuits for 2- and 3-bit A/D's were designed with GaAs MESFET's. Computer simulations showed that these circuits can function at or above 1.0-GHz sampling rates. Monolithic IC's were fabricated and evaluated. These IC's were successfully operated at GHz sampling rates. The sampling rate is the highest reported in the literature for devices operating at room temperature. These experimental results are in good agreement with the computer simulations. Further studies are underway to improve the sensitivity of the comparators and extend the design to 4-bit A/D's operating at GHz sampling rates.

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